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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yuji SATO

Application No.: New U.S. Patent Application

Filed: March 30, 2001 Docket No.: 108842

For: DATA TRANSFER DEVICE AND PRINTING APPARATUS INCLUDING THE SAME

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please replace paragraphs **[0033] and [0036] - [0039]** as follows:

[0033] When the system clock generating circuit 40 in FIG. 2 supplies a 48 MHz system clock (see FIG. 3) to the system clock input part 5, a system clock cycle becomes $1/(48 \times 10^6)$ seconds. The system clock is input to the transfer clock circuit 6 and the clock terminals 13b, 14b, 15b, 16b of the flip-flop 13, 14, 15, 16, respectively, as described above. The transfer clock circuit 6 performs 1/10 frequency division for the system clock, to generate the pre-delayed clock. The pre-delayed clock (see FIG. 2) with a cycle of $1/(48 \times 10^5)$ seconds are output from the output part 6b of the transfer clock circuit 6.